2. The finFET of claim 1 wherein the at least one trapping region traps ions produced by radiation incident on the substrate.

3. The finFET of claim 1 further comprising a field oxide formed in the channel above the elongated region.

4. The finFET of claim 1 wherein the elongated trapping region is reverse-biased relative to the substrate.

5. The finFET of claim 1 wherein the elongated trapping region is a defect region.

6. The finFET of claim 1 wherein the elongated trapping region is an epitaxial region formed on the substrate.

7. The finFET of claim 1 wherein the elongated trapping region is an epitaxial region formed on the substrate, the epitaxial region having a second conductivity type.

8. A finFET comprising:

a substrate of semiconductor material;

a first well region formed in the substrate and having p-type conductivity;

a plurality of first thin segments of the semiconductor material integral with the first well region and extending in a first direction away from the substrate, each first thin segment extending lengthwise in a second direction with a channel between adjacent first thin segments;

a transistor formed on each of at least two adjacent first thin segments, each transistor having source and drain regions and a gate;

at least one elongated first trapping region located in or on the substrate between two adjacent first thin segments, at least one of the elongated first trapping regions having n-type conductivity and being coupled to a well region having n-type conductivity;

a second well region formed in the substrate and having n-type conductivity;

a plurality of second thin segments of the semiconductor material integral with the second well region and extending in the first direction away from the substrate, each second thin segment extending lengthwise in the second direction with a channel between adjacent second thin segments;

a transistor formed on each of at least two adjacent second thin segments, each transistor having source and drain regions and a gate; and

at least one elongated second trapping region located in or on the substrate between two adjacent second thin segments, at least one of the elongated second trapping regions having p-type conductivity and being coupled to a well region having p-type conductivity.

9. The finFET of claim 8 wherein at least one of the first and second trapping regions traps ions produced by radiation incident on the substrate.

10. The finFET of claim 8 wherein at least one of the elongated first trapping regions has n-type conductivity type and at least one of the elongated second trapping regions has p-type conductivity.

11. The finFET of claim 10 wherein the elongated first and second trapping regions are reverse-biased.

12. The finFET of claim 8 wherein the elongated first and second trapping regions are defect regions.

13. The finFET of claim 8 wherein the elongated first and second trapping regions are epitaxial regions formed on the substrate.

14. A method for forming a finFET comprising:

forming a plurality of first thin semiconductor segments that are integral with a semiconductor substrate having a first conductivity type and are spaced apart by first channels;

forming in or on the substrate at a bottom of at least one first channel a first trapping region, by epitaxially growing on the substrate a region having a second conductivity-type opposite the first conductivity-type; and

forming in at least one first thin segment a transistor having source and drain regions and a gate.

15. The method of claim 14 wherein the first trapping region is formed by implanting ions having a second conductivity-type opposite the first conductivity-type.

16. The method of claim 14 further comprising the step of forming the first trapping region by implanting ions having sufficient energy to destroy some of the crystalline structure of the substrate.

17. The method of claim 14 wherein first thin semiconductor segments are integral with a first well region in the semiconductor substrate, the first well region having p-type conductivity, further comprising:

forming a plurality of second thin semiconductor segments that are integral with a second well region in the semiconductor substrate and are spaced apart by second channels, the second well region having n-type conductivity;

forming in or on the substrate at a bottom of at least one second channel a second trapping region; and

forming in at least one second thin segment a transistor having source and drain regions and a gate.

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